Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1-23 are withdrawn.

24. (New) A processor, comprising:

multiple multi-threaded engines integrated on a single semiconductor chip;

a random access memory integrated on the same semiconductor chip; and

a first memory controller integrated on the same semiconductor chip, the memory controller coupled to the random access memory and coupled to the multiple multi-threaded engines, the memory controller to receive and respond to commands issued by the multiple multi-threaded engines.

25. (New) The processor of claim 24,

wherein the commands received by the first memory controller comprise at least one command specifying bit-wise operations on a location within the random access memory.

26. (New) The processor of claim 24,

wherein the commands received by the first memory controller comprise at least one test-and-set command.

27. (New) The processor of claim 24,

further comprising a single-threaded processor integrated on the same semiconductor chip, the single-threaded processor having a different architecture than at least one of the multiple multi-threaded engines.

28. (New) The processor of claim 24, further comprising a host interface integrated on the same semiconductor chip.

29. (New) The processor of claim 28, wherein the host interface comprises a Peripheral Component Interconnect (PCI) interface.

30. (New) The processor of claim 24, further comprising an interface that is integrated on the same semiconductor chip, the interface comprising an interface to a network component to send and receive packets.

31. (New) The processor of claim 30, wherein the interface comprises an interface to a link layer device.

32. (New) The processor of claim 31, wherein the interface comprises an interface to a bus coupling the network component to the processor.

33. (New) The processor of claim 24, further comprising a second memory controller integrated on the same semiconductor chip, the second memory controller to interface to a random access memory not integrated on the same semiconductor chip, the second memory controller coupled to the multiple multi-threaded engines and to receive and respond to commands received from the multiple multi-threaded engines.

34. (New) The processor of claim 24, further comprising dedicated hash logic integrated on the same semiconductor chip, the dedicated hash logic coupled to the multiple multi-threaded engines.

35. (New) The processor of claim 24, wherein each of the multiple multi-threaded engines comprises:

an instruction control store to store instructions associated with multiple threads;

registers to store multiple contexts respectively associated with the multiple threads, each context comprising a program counter identifying an execution location within a one of the associated threads; and

an arbiter to select a one of the program counters associated with a one of the threads to execute.

36. (New) The processor of claim 24, further comprising:

a host interface integrated on the same semiconductor chip;

an interface, integrated on the same semiconductor chip, to a network component to send and receive packets; and

a second memory controller integrated on the same semiconductor chip, the second memory controller to interface to a random access memory not integrated on the same semiconductor chip, the second memory controller coupled to the multiple multi-threaded engines and to receive and respond to commands received from the multiple multi-threaded engines.